

KWABENA ADU BOAHEN

Address

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Bioengineering Department	Fax: (650) 736 8368
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Education

PhD, Computation & Neural Systems, <i>California Institute of Technology</i> , Pasadena CA	May 1997
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Thesis: *Retinomorphing Vision Systems: Reverse Engineering the Vertebrate Retina*

Advisor: *Prof. Carver Mead*

MSE, Electrical & Computer Engineering, <i>Johns Hopkins University</i> , Baltimore MD	June 1989
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BSE, Electrical & Computer Engineering, <i>Johns Hopkins University</i> , Baltimore MD	June 1989
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Positions

Stanford University, Stanford CA

Professor of Bioengineering & Electrical Engineering	2014-
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Director, <i>Brains in Silicon</i> Laboratory	2006-
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Associate Professor of Bioengineering (with tenure)	2006-2014
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University of Pennsylvania, Philadelphia PA

Associate Professor of Bioengineering (with tenure)	2003-2005
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Assistant Professor of Bioengineering	1997-2003
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Assistant Professor of Electrical Engineering	1997-2003
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Distinctions

Awards

National Institutes of Health, Director's Transformative R01 Award (<i>TR01</i>)	2011-2016
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National Institutes of Health, Director's Pioneer Award (<i>Pioneer</i>)	2006-2011
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Office of Naval Research, Young Investigator Program (<i>ONR YIP</i>)	2002-2005
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National Science Foundation, Faculty Early Career Program (<i>NSF CAREER</i>)	2001-2006
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Fellowships

Packard Foundation, Fellowships in Science and Engineering	1999-2004
Junior Chair, Skirkanich Term Asst. Prof., <i>University of Pennsylvania</i>	1997-2003
Caltech Sloan Center for Theoretical Neurobiology	1995-96

Honors

Fellow, American Institute for Medical and Biological Engineering (AIMBE)	2016
Fellow, Institute of Electrical and Electronic Engineers (IEEE)	2016
Advances in Neural Information Processing Systems 15, Best Student Paper Award	2003
38 th Midwest Symposium on Circuits & Systems, Myril B. Reed Best Paper Award	1995
Hopkins Concurrent MSE/BSE Program	1989
AT&T Information Systems Inc. Excellence Award	1989
Tau Beta Pi Engineering Honor Society	1987-Present

Professional Activities

Keynote/Plenary Addresses

<i>American Institute for Medical and Biological Engineering Annual Event, Washington DC</i>	2015
<i>Biophysical Society 57th Annual Meeting, Philadelphia PA</i>	2013
<i>10th Annual Computational Systems Neuroscience Meeting (Cosyne), Salt Lake City UT</i>	2013
<i>The 55th Midwest Symposium on Circuits and Systems, Boise ID</i>	2012
<i>IEEE Internatl. Symposium on Asynchronous Circuits and Systems, Lynby DENMARK</i>	2012
<i>5th International IEEE EMBS Conference on Neural Engineering, Cancun, MEXICO</i>	2011

Guest Editor

<i>IEEE Proceedings, Special Issue on “Engineering intelligent electronic systems based on computational neuroscience”</i>	2012-14
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Associate Editor

Neural Computation	2015-
Journal of Neural Engineering	2013-16
Frontiers in Neuromorphic Engineering	2010-

Chair

NSF Waterman Award Selection Committee	2009-10
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Reviewer

NIH Director's Pioneer Award	2012
IEEE Journal of Solid-State Circuits	2012
NIH Director's Early Independence Award (Editor for Stage 2)	2011-13
Proceedings of the National Academy of Sciences	2011
NIH Director's New Innovator Award	2009
IEEE Transactions on Biological Circuits and Systems	2008
NSF Waterman Award Selection Committee	2006-09
NSF/CISE Emerging Models and Technologies Program	2006
NSF/CISE-ECS CAREER Program	2005
IEEE Transactions in VLSI	2004-9
Science	2003
IEEE/EMBS Conf. on Neural Engineering	2002
IEEE Transactions on Neural Networks	2002-8
IEEE Transactions on Pattern Analysis and Machine Intelligence	2002
IEEE Transactions on Circuits and Systems I & II	2002-6
NSF Information Technology Research (ITR) Program	2001
NSF/IBN Computational Neuroscience Program	2000
nature	2000
Conference on Advanced Research in VLSI	1999
IEEE Circuits & Systems Technical Committee on Neural Systems	1997
Neural Information Processing Systems Conference	1997
Neural Computation	1995-Present

Program Committee

Neuromorphic Cognition Engineering Workshop, Telluride CO	2011-12
Neural Information Processing Systems Conference	2009

Session Chair

IEEE/EMBS Conference: Session on Neural Circuits—Biological and Artificial.	2003
NSF/DOE Workshop on Biological Information Processing	2001

Conference on Microelectronics for Neural, Fuzzy, Bioinspired Systems	1999
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Consultant

Tanner Research Inc., Pasadena CA	1994
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Synaptics Inc., San Jose CA	1992
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Institutional Activities

Stanford University, Stanford CA

Co-Chair, Joint SNI-BioE Junior Faculty Search Committee	2014-15
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Member, Interschool Theoretical Neuroscience Search Committee	2012
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Member, Neurosurgery Faculty Computational Neuroscience Search Committee	2012
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Associate Chair, Graduate Admissions, Bioengineering Dept.	2010-
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Chair, Bioengineering Faculty Search Committee	2008-9
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Member, Graduate Admissions Committee, Bioengineering Dept.	2006-9
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Member, Computer Science Faculty Search Committee	2008
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Member, Joint Bioengineering–Electrical Engineering Faculty Search Committee	2006-7
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University of Pennsylvania, Philadelphia PA

Internal Advisory Committee, Institute for Neurological Sciences	2003-05
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Executive Committee, Institute for Medicine and Engineering	2002-05
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Member, Bioengineering Faculty Search Committee	2000-04
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Advisor, Bioengineering Undergraduates (18 current students)	1998-05
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Director, Bioengineering PhD Qualifying Exams	1998-04
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Member, Neuroscience Graduate Group	1997-05
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Member, Institute for Neurological Studies	1997-05
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Member, Institute for Medicine and Engineering	1997-05
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University of Southern California, Los Angeles CA

Scientific Advisor, Biomimetic Microelectronic Systems NSF ERC	2003-09
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Teaching Experience

Stanford University, Stanford CA

Professor, BIOE123 – Optics and Devices Lab	Winter 2013-
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Professor, BIOE313/EE304 – Neuromorphics: Brains in Silicon	Spring 2013-
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Professor, BIOE301C – Diagnostic Devices Laboratory	Spring 2009-13
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Professor, BIOE332 – Large-Scale Neural Modeling	Winter 2009-13
Professor, BIOE332A,B – Large-Scale Neural Modeling	Winter, Spring 2007-09
<i>University of Pennsylvania, Philadelphia PA</i>	
Professor, BE511 – Biosystems	Spring 2003
Professor, BE526 – Neuromorphing: Building Brains in Silicon	Spring 1998-05
Professor, BE301 – Bioengineering Signals and Systems	Fall 98, Spring 00-02,04-05
<i>Neuromorphic Engineering Workshop, Telluride CO</i>	
Lecturer, Designing and Testing Asynchronous Circuits	June/July 2007-08
Lecturer, Configurable Neuromorphic Systems	June/July 2002-05
Lecturer, Asynchronous Interchip Communication using Address-Events	June/July 1998-2001
Lecturer, Multichip Neuromorphic Systems	June/July 1994-1998

Research Funding

Pending

None

Current

1. “Neuromorphics: Programmable Analog Computation through Probabilistic Digital Communication”, PI, \$1.022M year for 5 years, \$5.11M total. *Office of Naval Research*, with Chris Eliasmith (Systems Design Engineering, Waterloo, Co-PI) and Rajit Manohar (Computer Science, Cornell, Co-PI). Awarded April 2013
2. “Fully Implantable and Programmable Spike-Based Codecs for Neuroprosthetics”, PI, \$900,000/year for 5 years, \$4.5M total. *Transformative R01 Award*, with Krishna Shenoy (Elect. Eng., Stanford, Co-PI). Awarded July 2011

Past

3. “The Emergence of Attention From the Neural Circuitry of Sensorimotor Interactions: Combined Theoretical, Modeling and Experimental Approaches”, Co-PI, \$175,000/year for 2 years, \$350,000 total, *Stanford Bio-X Neuroventures Grant Program*, with Tirin Moore (Neurobiology, Stanford) and Surya Ganguli (Applied Physics, Stanford). Awarded May 2012
4. “Neuromorphic Circuits in 65nm CMOS”, PI, \$100,000/year for 3 years, \$300,000 total. *Samsung Advanced Institute of Technology’s Global Research Outreach Program*. Awarded January 2010
5. “Neurogrid: Emulating a million neurons in the cortex”, PI, \$780,000/year for 5 years, \$3.9M total. *NIH Director’s Pioneer Award*. Awarded Sept 2006
6. “Cognitive Computing via Synaptronics and Supercomputing”, Co-PI, \$143,845 for 9 months. *DARPA/DSO SyNAPSE Program*. Awarded October 2008.

7. "SEER: A gigascale neuromorphic visual system", PI, \$200,000/year for 3 years, \$600,000 total. *NSF EMT Program*, with Yiannis Aloimonos (Comp. Sci., Maryland). Awarded August 2005
8. "Spontaneous activity, lateral interactions, and cortical maps", PI, \$286,974/year for 3 years, \$860,921 total. *NIH NIMH ROI*, with Matthew Dalva (Neurosci., PENN), Marcos Frank (Neurosci., PENN), and Geoffrey Goodhill (Neurosci., U. Queensland, AUSTRALIA). Awarded July 2004
9. "Neuromorphic Episodic Memories", PI, \$105,000/year for 3 years, \$315,000 total. *ONR YIP Program*. Awarded Feb 2002
10. "Bayesian Hypercolumns for Intelligent Image Analysis," Co-PI, \$600,000/year for 5 years, \$3,000,000 total. *DOD/ONR FY2001 MURI Program*, with Leif Finkel (BE, UPenn, PI), Paul Sajda (BE, Columbia), Edward Adelson (BCS, MIT), Diego Contreras (Neurosci, UPenn), and Ike Bendall (SPAWAR). Awarded Feb 2001
11. "Neuromorphic Computation *in Silico*," PI, \$75,000/year for 5 years, \$375,000 total. *NSF CAREER Program*. Awarded Feb 2001
12. "Epigenetic Computers: An *in vitro*, *in abstractio*, and *in silico* study", PI, \$326,000/year for 3 years, \$980,000 total. *NSF BITS Program*, with Rita Balice-Gordon (Neurosci, UPenn), Geoff Goodhill (Neurosci, Georgetown), and Bertram Shi (EE, HKUST). Awarded Sept 2001
13. "Meso-Scale Optical Imaging of Perceptual Learning," Co-PI, \$200,000/year for 5 years, \$1,000,000 total. *David & Lucile Packard Interdisciplinary Science Program*, with Leif Finkel (BE, PI), Diego Contreras (Neurosci), Arjun Yodh (Physics) & Brian Salzberg (Neurosci). Awarded July 2000
14. "Learning as you grow: Neuromorphic chips that rewire themselves," PI, \$125,000/year for 5 years, \$625,000 total. *The David & Lucile Packard Foundation*. Awarded October 1999
15. "Retinomorph Vision Chips for Ocular Implants," PI, \$70,000/year for 3 years, \$210,000 total. *The Whitaker Foundation*, Rosslyn VA. Awarded January 1999
16. "Neuromorphic Knowledge Systems," Co-PI, \$533,000/year for 3 years, \$1,600,000 total. *NSF-Knowledge and Distributed Intelligence Program*, with Leif Finkel (BE), George Gerstein (Neuroscience), and John Hopfield (Princeton). Awarded October 1998
17. "Virtual Integration for Autonomous Microrobots", PI, \$19,900/year for 1 year, \$19,900 total. *NASA Neurotechnology Program*. Awarded Aug 1998
18. "A Visual Prosthesis: Creating an Artificial Retina", PI, \$14,855/year for 1 year, \$14,855 total. *Lindback Foundation: Minority Junior Faculty Grants*. Awarded May 1998

Refereed Journal Publications

1. A Neckar, S Fok, B Benjamin, T Stewart, N Oza, C Eliasmith, R Manohar, and **K Boahen**, "Braindrop: A Mixed-Signal Neuromorphic Architecture with a Dynamical Systems-Based Programming Model", *Proceedings of the IEEE*. Submitted
2. **K Boahen**, "A Neuromorph's Prospectus", *Computing in Science & Engineering*, vol 19, no 2, pp 14-28, IEEE Computer Society, Los Alamitos CA, USA, 2017.
3. T A Engel, N A Steinmetz, M A Gieselmann, A Thiele, T Moore, and **K Boahen**, "Selective modulation of cortical state during spatial attention", *Science*, vol 354, no 6316, pp 1140-1144, 2016.
4. B V Benjamin, P Gao, E McQuinn, S Choudhary, A R Chandrasekaran, J-M Bussat, R Alvarez-Icaza, J V Arthur, P Merolla, and **K Boahen**, "Neurogrid: A Mixed-Analog-Digital Multichip System for Large-Scale Neural Simulations", *Proceedings of the IEEE*, vol 102, no 5, pp 699-716, 2014.
4. P Merolla, J V Arthur, R Alvarez-Icaza, J-M Bussat, and **K Boahen**, "A Multicast Tree Router for Multichip Neuromorphic Systems", *IEEE Transactions on Circuits and Systems*, vol 61, no 3, pp 820-833, 2014.
5. J H Wittig and **K Boahen**, "Potassium conductance dynamics confer robust spike-time precision in a neuromorphic model of the auditory brainstem", *Journal of Neurophysiology*, vol 110, pp 307-21, 2013.
6. J Dethier, P Nuyujukian, S I Ryu, K V Shenoy, and **K Boahen**, "Design and Validation of a Real-Time Spiking-Neural-Network Decoder for Brain-Machine Interfaces", *Journal of Neural Engineering*, vol 10, no 3, 036008, 12 pp, 2013.
7. R Alvarez-Icaza and **K Boahen**, "Inferior Olive Mirrors Joint Dynamics to Implement an Inverse Controller", *Biological Cybernetics*, vol 106 issue 8-9, pp 429-39, 2012
8. P Gao, B V Benjamin and **K Boahen**, "Dynamical system guided mapping of quantitative neuronal models onto neuromorphic hardware", *IEEE Transactions on Circuits and Systems*, Vol 59, no 10, pp 2383-94, Oct 2012.
9. R Alvarez-Icaza and **K Boahen**, "Deep cerebellar neurons mirror the spinal cord's gain to implement an inverse controller", *Biological Cybernetics*, vol 105 issue 1, pp 29-40, August 2011.
10. G Indiveri, B Linares-Barranco, T J Hamilton, A van Schaik, R Etienne-Cummings, T Delbruck, S-C Liu, P Dudek, P Hafliger, S Renaud, J Schemmel, G Cauwenberghs, J Arthur, K Hynna, F Folowosele, S Saighi, T Serrano-Gotarredona, J Wijekoon, Y Wang, and **K Boahen**, "Neuromorphic silicon neuron circuits", *Frontiers in Neuroscience*, vol 5, no 73, May 2011.
11. D Sridharan, **K Boahen** and E Knudsen, "Space Coding by Gamma Oscillations in the Barn Owl Optic Tectum ", *J Neurophys.* vol 105, pp 2005-2017, May 2011.
12. J V Arthur and **K Boahen**, "Silicon-Neuron Design: The Dynamical Systems Approach", *IEEE Transactions on Circuits and Systems*, vol 58, no 5, pp 1034-1043, May 2011.
13. B Wen and **K Boahen**, "A Silicon Cochlea with Active Coupling", *IEEE Transactions on Biomedical Circuits and Systems*, vol 3, no 6, pp 444-455, December 2009.
14. K M Hynna and **K Boahen**, "Nonlinear Influence of T-Channels in an *in-silico* Relay Neuron", *IEEE Transactions on Biomedical Engineering*, vol 56, no 6, pp 1734-43, June 2009.
15. R Silver, **K Boahen**, S Grillner, N Kopell and K L Olsen, "Neurotech for neuroscience: Unifying concepts, organizing principles, and emerging tools", *Journal of Neuroscience*, vol 27, no 44, pp 11807-819, October 2007.

16. K A Zaghloul, M Manookin, B Borghuis, **K Boahen** and J B Demb, "Functional circuitry for peripheral suppression in mammalian Y-type ganglion cells", *Journal of Neurophysiology*, vol 97, no 6, pp 4327-4340, June 2007.
17. J V Arthur and **K Boahen**, "Synchrony in Silicon: The Gamma Rhythm", *IEEE Transactions on Neural Networks*, vol 18, no 6, pp 1815-1825, November 2007.
18. K M Hynna and **K Boahen**, "Thermodynamically-Equivalent Silicon Models of Ion Channels", *Neural Computation*, vol 19, no 2, pp 327-350, February 2007
19. P Merolla, J Arthur, B E Shi and **K Boahen**, "Expandable Networks for Neuromorphic Chips", *IEEE Transactions on Circuits and Systems I*, vol 54, No 2. pp. 301-311, February 2007.
20. K A Zaghloul and **K Boahen**, "A silicon retina that reproduces signals in the optic nerve", *Journal of Neural Engineering*, vol 3, no 4, pp 257-267, December 2006
21. T Y W Choi, P Merolla, J Arthur, **K Boahen** and B E Shi, "Neuromorphic Implementation of Orientation Hypercolumns", *IEEE Transactions on Circuits and Systems I*, vol 52, no 6, pp 1049-1060, June 2005.
22. K A Zaghloul, **K Boahen** and J B Demb, "Contrast Adaptation in Subthreshold and Spike Responses of Mammalian Y-Type Retinal Ganglion Cells", *Journal of Neuroscience*, vol 25, no 4, pp 860-868, January 2005.
23. K A Zaghloul and **K Boahen**, "An On-Off Log-Domain Circuit that Recreates Adaptive Filtering in the Retina", *IEEE Transactions on Circuits and Systems I*, vol 52, no 1, pp 99-107, January 2005.
24. **K Boahen**, "A Burst-Mode Word-Serial Address-Event Link—III: Analysis and Testing", *IEEE Transactions on Circuits and Systems I*, vol 51, no 7, pp 1292-1300, July 2004.
25. **K Boahen**, "A Burst-Mode Word-Serial Address-Event Link—II: Receiver Design", *IEEE Transactions on Circuits and Systems I*, vol 51, no 7, pp 1281-1291, July 2004.
26. **K Boahen**, "A Burst-Mode Word-Serial Address-Event Link—I: Transmitter Design", *IEEE Transactions on Circuits and Systems I*, vol 51, no 7, pp 1269-1280, July 2004.
27. K A Zaghloul and **K Boahen**, "Optic Nerve Signals in a Neuromorphic Chip I: Outer and Inner Retina Models", *IEEE Transactions on Biomedical Engineering*, vol 51 no 4, pp 657-666, 2004.
28. K A Zaghloul and **K Boahen**, "Optic Nerve Signals in a Neuromorphic Chip II: Testing and Results", *IEEE Transactions on Biomedical Engineering*, vol 51 no 4, pp 667-675, 2004.
29. T Y W Choi, B E Shi, and **K Boahen**, "An ON-OFF Orientation Selective Address Event Representation Image Transceiver Chip", *IEEE Transactions on Circuits and Systems I*, vol 51, no 2, pp 342-353, 2004.
30. K A Zaghloul, **K Boahen**, and J B Demb, "Different Circuits for ON and OFF Retinal Ganglion Cells cause Different Contrast Sensitivities", *Journal of Neuroscience*, vol 23, no 7, pp. 2645-2654, April 2003.
31. E Culurciello, R Etienne-Cummings, and **K Boahen**, "A Biomorphic Digital Image Sensor", *IEEE Journal of Solid State Circuits*, vol 38, no 2, pp 281-294, 2003.
32. B E Shi and **K Boahen**, "Competitively Coupled Orientation Selective Cellular Neural Networks", *IEEE Transactions on Circuits and Systems I*, vol 49, no 3, pp388-394, 2002.

33. **K Boahen**, "A Retinomorph Chip with Parallel Pathways: Encoding ON, OFF, INCREASING, and DECREASING Visual Signals", *Journal of Analog Integrated Circuits and Signal Processing*, vol 30, no 2, pp 121-135, 2002. Invited paper
34. E Culurciello, R Etienne-Cummings, and **K Boahen**, "Arbitrated Address-Event Representation Digital Image Sensor", *Electronics Letters*, vol 37, no 24, pp 1443-1445, 2001.
35. K Hynna and **K Boahen**, "Space-Rate Coding in an Adaptive Silicon Neuron", *Neural Networks*, Special Issue on *Spiking Neurons in Neuroscience and Technology*, vol 14, no 6-7, pp 645-656, 2001. Invited paper
36. **K A Boahen**, "Point-to-Point Connectivity Between Neuromorphic Chips using Address-Events", *IEEE Transactions on Circuits & Systems II*, vol 47 no 5, pp 416-434, 2000. Invited Paper
37. **K A Boahen**, "The Retinomorph Approach: Adaptive Pixel-Parallel Amplification, Filtering, and Quantization", *Journal of Analog Integrated Circuits and Signal Processing*, vol 13, no 1-2, pp 53-68, 1997.
38. A G Andreou and **K A Boahen**, "Translinear Circuits in Subthreshold MOS", *Journal of Analog Integrated Circuits and Signal Processing*, vol 9, pp 141-166, 1996.
39. A G Andreou, R C Meitzler, K Strohbehn, and **K A Boahen**, "Analog VLSI Neuromorphic Image Acquisition and Preprocessing Systems", *Neural Networks*, vol 8, pp 1323-1347, 1995.
40. A G Andreou, **K A Boahen**, et. al., "Current-Mode Subthreshold MOS Circuits for Analog VLSI Neural Systems", *IEEE Trans. on Neural Networks*, vol 2, no 2, pp 205-213, 1991.
41. A G Andreou and **K A Boahen**, "Synthetic Neural Circuits using Current-Domain Signal Representations", *Neural Computation*, vol 1, pp 489-501, 1989.
42. **K A Boahen**, P O Pouliquen, et. al., "A Heteroassociative Memory using Current-Mode MOS Analog VLSI Circuits", *IEEE Trans. on Circuits and Systems*, vol 36, no 5, pp 747-755, 1989.

Book Chapters

1. B Wen and **K Boahen**, "A Biomorphic Active Cochlear Model *In Silico*", *Integrated Microsystems: Electronics, Photonics, and Biotechnology*, K Iniewski, Ed., ch 10, pp 207-235, CRC Press, Boca Raton FL, 2011. Invited chapter
2. K A Zaghoul and **K Boahen**, "Circuit Designs that Model the Properties of the Outer and Inner Retina", *Visual Prosthetics and Ophthalmic Devices: New Hope in Sight*, J Tombran-Tink & C J Barnstable, Eds., ch 10, pp 135-158, 2007. Invited chapter
3. **K A Boahen**, "Communicating Neuronal Ensembles between Neuromorphic Chips", *Neuromorphic Systems Engineering*, T S Lande, Ed, ch 11, pp 229-261, Kluwer Academic Publishers, Boston MA, 1998.
4. **K A Boahen**, "The Retinomorph Approach: Pixel-Parallel Adaptive Amplification, Filtering, and Quantization," *Neuromorphic Systems Engineering*, T S Lande, Ed, ch 5, pp 131-152, Kluwer Academic Publishers, Boston MA, 1998.
5. A G Andreou and **K A Boahen**, "Neural Information Processing II", *Analog VLSI: Signal and Information Processing*, M Ismail and T Fiez, Eds, ch 8, pp 358-413, McGraw-Hill, New York, 1994.

6. **K A Boahen** and A G Andreou, "Design of a Bidirectional Associative Memory Chip", *Associative Neural Memories: Theory and Implementation*, M. Hassoun, Ed, ch 17, pp 288-305, Oxford Univ. Press, New York, 1993.

Refereed Conference Publications

1. A Neckar, T Stewart, B Benjamin, and K Boahen, "Optimizing an Analog Neuron Circuit Design for Nonlinear Function Approximation", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence ITALY, 2018. Accepted
1. A R Voelker, B V Benjamin, T C Stewart, **K Boahen**, and C Eliasmith, "Extending the Neural Engineering Framework for Nonideal Silicon Synapses", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore MD, 2017.
2. E Kauderer-Abrams and **K Boahen**, "Calibrating Silicon-Synapse Dynamics using Time-Encoding and Decoding Machines", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore MD, 2017.
3. E Kauderer-Abrams, A Gilbert, A Voelker, B Benjamin, and T C Stewart, and **K Boahen**, "A Population-Level Approach to Temperature Robustness in Neuromorphic Systems", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore MD, 2017.
4. A Cutkosky and **K Boahen**, "Online Convex Optimization with Unconstrained Domains and Losses", *Advances in Neural Information Processing Systems (NIPS-29)*, Barcelona SPAIN, 2016.
5. A Cutkosky and **K Boahen**, Bloom Features, *IEEE International Conference on Computation Science and Computational Intelligence*, IEEE Computer Society, pp 547-552, 2015.
6. S Menon, S Fok, A Neckar, O Khatib, and **K Boahen**, "Controlling Articulated Robots in Task-Space with Spiking Silicon Neurons", *5th IEEE RAS & EMBS International Conference on Biomedical Robotics and Biomechatronics (BioRob)*, IEEE Press, pp 181-186, 2014.
7. S Choudhary, S Sloan, S Fok, A Neckar, E Trautmann, P Gao, T Stewart, C Eliasmith, and **K Boahen**, "Silicon Neurons that Compute", *International Conference on Artificial Neural Networks*, LNCS vol 7552, pp 121-28, Springer, Heidelberg, 2012.
8. B V Benjamin, J V Authur, P Gao, P Merolla and **K Boahen**, "A Superposable Silicon Synapse with Programmable Reversal Potential", *Annual International Conference of the IEEE Engineering and Medicine in Biology Society (EMBC)*, pp 771-4, 2012.
9. J Dethier, P Nuyujukian, C Eliasmith, T Stewart, S A Elassaad, K V Shenoy, and **K Boahen**, "A Brain-Machine Interface Operating with a Real-Time Spiking Neural Network Control Algorithm", *Advances in Neural Information Processing Systems 24*, J Shawe-Taylor, R S Zemel, P Bartlett, F C N Pereira & K Q Weinberger, Eds., Curran Associates, Inc., pp 2213-21, 2011.
10. J Dethier, V Gilja, P Nuyujukian, S A Elassaad, K V Shenoy, and **K Boahen**, "Spiking Neural Network Decoder for Brain-Machine Interfaces", *IEEE EMBS 5th Intl. Conference on Neural Engineering*, IEEE Press, pp 369-399, 2011.
11. A Chandrasekaran and **K Boahen**, "A 1-change-in-4 Delay-Insensitive Interchip Link", *IEEE International Symposium on Circuits and Systems*, IEEE Press, pp 3216-3219, 2010.
12. J Lin and **K Boahen**, "A Delay-Insensitive Address-Event Link", *15th IEEE Symposium on Asynchronous Circuits and Systems*, IEEE Press, pp 55-62, 2009.

13. D Sridharan, B Percival, J Arthur and **K Boahen**, "An *in-silico* Neural Model of Dynamic Routing through Neuronal Coherence", *Advances in Neural Information Processing Systems 20*, J C Platt, D Koller, Y Singer and S Roweis Eds., MIT Press, pp 1401-1408, 2008.
14. K M Hynna and **K Boahen**, "Silicon Neurons that Burst when Primed", *IEEE International Symposium on Circuits and Systems*, IEEE Press, pp 3363-3366, 2007.
15. J Lin, P Merolla, J Arthur and **K Boahen**, "Programmable Connections in Neuromorphic Grids", *49th IEEE Midwest Symposium on Circuits and Systems*, vol 1, pp 80-84, IEEE Press, 2006.
16. J H Wittig Jr. and **K Boahen**, "Silicon Neurons that Phase-Lock", *IEEE International Symposium on Circuits and Systems*, IEEE Press, pp 4535-4538, 2006.
17. P A Merolla and **K Boahen**, "Dynamic Computation in a Recurrent Network of Heterogeneous Silicon Neurons", *IEEE International Symposium on Circuits and Systems*, IEEE Press, pp 4539-4542, 2006.
18. K M Hynna and **K Boahen**, "Neuronal Ion-Channel Dynamics in Silicon", *IEEE International Symposium on Circuits and Systems*, IEEE Press, pp 3614-3617, 2006.
19. J V Arthur and **K Boahen**, "Silicon Neurons that Inhibit to Synchronize", *IEEE International Symposium on Circuits and Systems*, IEEE Press, pp 4807-4810, 2006.
20. B Wen and **K Boahen**, "A 360-Channel Speech Preprocessor that Emulates the Cochlear Amplifier", *IEEE International Solid-State Circuits Conference*, Digest of Technical Papers, pp 556-57, IEEE Press, 2006.
21. B Taba and **K Boahen**, "Silicon Growth Cones Map Silicon Retina", *Advances in Neural Information Processing Systems 18*, B Sholkopf and Y Weiss Eds., pp 1329-1336, MIT Press, 2006.
22. B Wen and **K Boahen**, "Active Bidirectional Coupling in a Cochlear Chip", *Advances in Neural Information Processing Systems 18*, B Sholkopf and Y Weiss Eds., pp 1497-1504, MIT Press, 2006.
23. J V Arthur and **K Boahen**, "Learning in Silicon: Timing is Everything", *Advances in Neural Information Processing Systems 18*, B Sholkopf and Y Weiss Eds., pp 75-82, MIT Press, 2006.
24. B Taba and **K Boahen**, "Balancing Guidance Range and Strength Optimizes Self-Organization by Silicon Growth Cones", *Artificial Neural Networks: Biological Inspirations – ICANN 2005: 15th International Conference*, W Duch, J Kacprzyk, E Oja, et al. Eds, LNCS 3697, pp 1027-1034, Springer-Verlag Berlin, 2005.
25. S Y M Lam, B E Shi and **K Boahen**, "Self-organized Cortical Map Formation by Guiding Connections", *IEEE International Symposium on Circuits and Systems*, pp 5230-5233, 2005.
26. J V Arthur and **K Boahen**, "Recurrently Connected Silicon Neurons with Active Dendrites for One-Shot Learning", *International Joint Conference on Neural Networks, IJCNN'04*, IEEE Press, pp 1699-1704, 2004.
27. P Merolla and **K Boahen**, "A Recurrent Model of Orientation Maps with Simple and Complex Cells", *Advances in Neural Information Processing Systems 16*, S Thrun, L Saul, and B Sholkopf Eds., MIT Press, pp 995-1002, 2004.

28. T Y W Choi, B E Shi, and **K Boahen**, "A Multi-Chip Model of Cortical Orientation Hypercolumns", *IEEE International Symposium on Circuits and Systems*, vol 3, pp 13-16, 2004.
29. K M Hynna and **K Boahen**, "A Silicon Implementation of the Thalamic Low Threshold Calcium Current", *International Conference of the IEEE Engineering and Medicine in Biology Society*, pp. 2228-2231, 2003.
30. B Wen and **K Boahen**, "A Linear Cochlear Model with Active Bi-directional Coupling", *International Conference of the IEEE Engineering and Medicine in Biology Society*, pp. 2013-2016, 2003.
31. B Taba and **K Boahen**, "Topographic Map Formation by Silicon Growth Cones", *Advances in Neural Information Processing Systems 15*, S Becker, S Thrun, and K Obermayer, Eds, MIT Press, pp. 1163-1170, 2003.
32. T Y W Choi, B E Shi, **K Boahen**, "An orientation selective 2D AER transceiver", *IEEE International Symposium on Circuits and Systems*, vol 4, pp xx-yy, 2003
33. B E Shi, T Y W Choi, and **K Boahen**, "On-Off Differential Current-Mode Circuits for Gabor-Type Spatial Filtering", *IEEE International Symposium on Circuits and Systems*, vol 2, pp 724-727, 2002.
34. E Culurciello, R Etienne-Cummings, and **K Boahen**, "High Dynamic-Range Arbitrated Address Event Representation Digital Imager", *IEEE International Symposium on Circuits and Systems*, vol 2, pp 505-508, 2001.
35. B E Shi and **K Boahen**, "Competitive Orientation Selective Arrays", Special Session on Gabor Filters and Transforms for Image Processing, *European Conference on Circuit Theory and Design*, pp 45-48, Espoo Finland, August 2001. Invited paper.
36. E Culurciello, R Etienne-Cummings, and **K Boahen**, "Arbitrated Address Event Representation Digital Image Sensor", *IEEE International Solid-State Circuits Conference*, pp 92-93, 2001.
37. **K A Boahen**, "Retinomorphic Chips that see Quadruple Images", *7th International Conference on Microelectronics for Neural, Fuzzy, and Bio-Inspired Systems (MicroNeuro '99)*, IEEE Computer Society Press, Los Alamitos CA, pp 12-20, 1999. Invited paper.
38. **K A Boahen**, "A Throughput-On-Demand Address-Event Transmitter for Neuromorphic Chips", *20th Anniversary Conference on Advanced Research in VLSI (ARVLSI'99)*, IEEE Computer Society Press, Los Alamitos CA, pp 72-86, 1999.
39. **K A Boahen**, "Retinomorphic Systems II: Communication Channel Design", *IEEE International Symposium on Circuits and System*, Supplement, pp 14-17, 1996.
40. **K A Boahen**, "Retinomorphic Systems I: Pixel Design", *IEEE International Symposium on Circuits and Systems*, Supplement, pp 9-13, 1996.
41. S-C Liu and **K A Boahen**, "Adaptive retina with center-surround receptive field", *Advances in Neural Information Processing Systems*, D S Touretzky, M C Mozer, and M E Hasselmo, Eds, vol 8, pp 678-684, MIT Press, Cambridge MA, 1996.
42. **K A Boahen**, "Retinomorphic Vision Systems", *Fifth International Conference on Microelectronics for Neural Networks and Fuzzy Systems (MicroNeuro '96)*, IEEE Computer Soc. Press, pp 2-14, 1996. Invited Paper

43. A G Andreou and **K A Boahen**, "A 590,000-Transistor, 48,000-Pixel Contrast-Sensitive, Edge-Enhancing CMOS Imager", *16th Conference on Advanced Research in VLSI (ARVLSI'95)*, pp 225-240, 1995.
44. A G Andreou and **K A Boahen**, "A 48,000-Pixel Silicon Retina in Current-Mode Subthreshold CMOS", *37th Midwest Symposium on Circuits and Systems*, vol 1, pp 97-102, 1994.
45. **K A Boahen** and A G Andreou, "A Contrast Sensitive Silicon Retina with Reciprocal Synapses", *Advances in Neural Information Processing Systems*, J E Moody and R P Lippmann, Eds, vol 4, pp 764-772, Morgan Kaufmann, San Mateo CA, 1992.
46. P O Pouliquen, **K A Boahen**, A G Andreou, "A Gray-code MOS current-mode analog-to-digital converter design", *IEEE International Symposium on Circuits and Systems*, vol 4, pp 1924-1927, 1991.
47. **K A Boahen**, A G Andreou, et al "Architectures for Associative Memories using Current-Mode MOS Circuits", *Advanced Research in VLSI*, C L Seitz Ed., MIT Press, Cambridge MA, 1989.

Miscellaneous Publications

1. **K Boahen**, "Neuromorphic Microchips", *Scientific American*, vol 292, no 5, pp 56-63, May 2005. [Invited Article](#)
2. **K A Boahen**, "A Retinomorph Vision System", *IEEE Micro*, vol 16, no 5, pp 30-39, 1996. [Invited Article](#)

Patents

1. **K A Boahen**, A G Andreou, P O Pouliquen, and R E Jenkins, "Current-Mode Based Analog Circuits for Synthetic Neural Systems", *United States Patent*, no 5,206,541, 27 Apr 1993.

Presentations

Talks: Conferences and Symposia

1. “Neuromorphic Chips: Addressing the Challenges of Nanoscale Transistors by Combining Analog Computation with Digital Communication”, *IEEE International Conference on Rebooting Computing (ICRC2016)*, San Diego CA. 2016
2. “Neuromorphic Chips: Combining Analog Computation with Digital Communication”, Fifth Annual Karles Invitational Conference on Neuroelectronics, Naval Research Laboratory (NRL), Washington, D.C. 2015
3. “Neurogrid: A hybrid analog-digital platform for simulating large-scale neural models”, *10th Annual Computational Systems Neuroscience Meeting (Cosyne)*, Salt Lake City UT. 2013
4. “Linking Cognition to Biophysics using a hybrid analog-digital simulator”*, *Biophysical Society 57th Annual Meeting*, Philadelphia PA. 2013
5. “Neurogrid: Simulating a million neurons and a billion synapses with sixteen neuromorphic chips”*, *Bernstein Conference on Computational Neuroscience*, Munich GERMANY. 2012
6. “Neurogrid: Simulating a million neurons and a billion synapses with sixteen neuromorphic chips”*, *34th Annual IEEE International Conference of the IEEE Engineering in Medicine & Biology Society*, San Diego CA. 2012
7. “Neurogrid: A mixed analog-digital multichip system for large-scale brain simulations”*, *The 55th Midwest Symposium on Circuits and Systems*, Boise ID. Keynote speaker 2012
8. “Neurogrid: A mixed-analog-digital multichip system for large-scale brain simulations”*, *IEEE International Symposium on Asynchronous Circuits and Systems*, Lynby DENMARK. Keynote speaker 2012
9. “Neurogrid: A mixed analog-digital multichip system for large-scale brain simulations”*, *What’s Next for Neuroscience? Insights from our Closest Relatives*, Janelia Farm, Ashburn VA. 2012
10. “Simulating a two-cortical area model of top-down attention on Neurogrid”*, *NIH Director’s Pioneer Award Symposium*, NIH, Bethesda MD. 2011
11. “Emulating a million neurons in the cortex”*, *18th Annual Joint Symposium on Neural Computation*, University of California, San Diego CA. Keynote speaker 2011
12. “Efficient high-performance computing for large-scale brain simulations using neuromorphic chips”*, *CMOS Emerging Technologies Meeting*, Whistler, CANADA. 2011
13. “Modeling the brain with neuromorphic chips”*, *5th International IEEE EMBS Conference on Neural Engineering*, Cancun, MEXICO. Plenary presentation 2011
14. “Neurogrid: Emulating a million neurons in the cortex”, *Dynamical Neuroscience XVIII*, San Diego CA. 2010
15. “Smart chips for emulating smart brains”*, *Brain Science 10th Anniversary Symposium*, Brown University, Providence RI. 2010

16. "Neurogrid: Emulating a million neurons in the cortex"*, *Neuro2010: Joint Conference of the Japanese Neuroscience, Neurochemistry, and Neural Network Societies*, Kobe JAPAN. 2010
17. "Neurogrid: Emulating a million neurons in the cortex"*, *Gordon Research Conference on the Neurobiology of Cognition*, Waterville Valley Resort NH. 2010
18. "Smart chips for modeling smart brains"*, *IEEE EMBS Forum on Grand Challenges in Neuroengineering*, Bethesda MD. 2010
19. "Neurogrid: Emulating a million neurons in the cortex"*, *Zurich Neuroscience Center (ZNZ) Symposium*, University of Zurich and Swiss Federal Institute of Technology (ETH), Honggerberg SWITZERLAND. 2009
20. "Googling the brain on a chip"*, *The Future of Human Health*, Stanford Homecoming Reunion, Stanford CA. 2008
21. "Emulating the brain in silicon"*, *Neuroscience 2007*, Annual Conference of the Society for Neuroscience, San Diego CA. 2007
22. "Neurogrid: Emulating a million neurons"*, *NIH Director's Pioneer Award Symposium*, NIH, Bethesda MD. 2007
23. "Emulating the brain"*, *TEDGlobal 2007*, Arusha TANZANIA. 2007
24. "The brain and the computer"*, *65th Device Research Conference (DRC)*, University of Notre Dame, South Bend, IN 2007
25. "Metaelectronics: Self-configuring neuromorphic systems"*, *Reflections | Projections 2006*, University of Illinois, Urbana IL 2006
26. "Neurogrid: Emulating a million neurons in the cortex"*, *EMBC06: Engineering in Medicine and Biology Conference*, Special Session on Applied Neural Computing, New York NY 2006
27. "Spontaneous activity, lateral interactions, and cortical maps", *CRCNS NIH/NSF Program PI Meeting*, Arlington VA. 2006
28. "Neuromorphic Electronics"*, IBM's 2006 Almaden Institute on Cognitive Computing, San Jose, CA. 2006
29. "Building neuromorphic systems by modeling developmental processes in silicon", *Penn: Past, present and future (Satellite of BMES2004)*, Philadelphia PA 2004
30. "How to build a brain", *NAE Regional Meeting*, School of Engineering and Applied Science, University of Pennsylvania, Philadelphia PA. 2004
31. "Morphing brains into microchips"*, *Undergraduate Symposium on Neural Systems*, Univ of Penn, Philadelphia PA 2002
32. "A Retinomorph chip with four types of ganglion cells", *Celebrating Frank Werblin's 35 Years of Retinal Research*, Berkeley CA 2001
33. "Retinomorph Vision Chips for Ocular Implants"*, *Biomedical Engineering Society Annual Meeting (BMES'00)*, Seattle WA 2000
34. "Spike coding in a retinomorph chip with four types of ganglion cells"*, *FASEB Retina Meeting*, Copper Mountain CO 2000

35. "Towards a Visual Prosthesis"*, *World Congress on Neurological Rehabilitation*, Toronto CANADA 1999
36. "Retinomorphics Chips that see Quadruple Images"*, *Conference on Microelectronics for Neural, Fuzzy, Bio-inspired Systems*, Granada SPAIN 1999
37. "A Throughput-On-Demand Address-Event Transmitter", *Conference on Advanced Research in VLSI*, Atlanta GA 1999
38. "Reverse Engineering the Vertebrate Retina"*, *3rd SONA International Conference*, Cape Town, SOUTH AFRICA 1997
39. "Retinomorphics Vision Systems"*, *Microelectronics for Neural Networks and Fuzzy Systems*, Lausanne, SWITZERLAND 1996
40. "Understanding Spatiotemporal Filtering in the Retina: A Silicon Model", *Computation & Neural Systems*, Boston MA 1996
41. "Retinomorphics Systems II: Communication Channel Design", *International Symposium on Circuits & Systems*, Atlanta GA 1996
42. "Retinomorphics Systems I: Pixel Design", *International Symposium on Circuits & Systems*, Atlanta GA 1996
43. "Speed Sensitivity in a Retinomorphics Chip"*, *FASEB Retina Meeting*, Saxtons River VM 1994
44. "A Contrast Sensitive Silicon Retina with Reciprocal Synapses", *Neural Information Processing Systems (NIPS-4)*, Denver CO 1991
45. "Architectures for Associative Memories using Current-Mode Analog MOS", *The Decennial Caltech Conference on VLSI*, Pasadena CA 1989

Lectures: Seminars and Colloquia (Invited)

1. "Neuromorphic Computing", *Capital Science Evening Lecture*, Carnegie Institution for Science, Washington DC. 2017
2. "Neuromorphic Computing", *12th Annual Coordinated Science Laboratory Student Conference*, University of Illinois, Urbana-Champaign IL (UIUC) 2017
3. "Neuromorphic Chips: Combining Analog Computation with Digital Communication", Department of Bioengineering, University of Pennsylvania, Philadelphia PA 2015
4. "Neuromorphic Chips: Combining Analog Computation with Digital Communication", Rockwood Lecture at UCSD, Institute for Neural Computation, University of California, San Diego CA (UCSD) 2015
5. "Neuromorphic Chips: Combining Analog Computation with Digital Communication", Computation and Neural Systems, California Institute of Technology (Caltech), Los Angeles CA 2015
6. "Neuromorphic Chips: Combining Analog Computation with Digital Communication", Department of Electrical Engineering, University of Southern California (USC), Los Angeles CA 2015
7. "Design and Application of Neuromorphic Chips", Stanford Linear Accelerator Center, Stanford CA. 2014

8. "Neuromorphic Architectures", Frankfurt Institute for Advanced Studies, University of Frankfurt, Frankfurt GERMANY. 2013
9. "Neurogrid: An energy-efficient platform for simulating large-scale neural models", Biomedical Engineering Department, Johns Hopkins University, Baltimore MD. 2013
10. "Neurogrid: A neuromorphic system with sixteen mixed analog-digital chips that models a million neurons and a billion synapses", Institute of Neuroinformatics, University of Zurich, Zurich, SWITZERLAND. 2012
11. "Simulating a two-cortical area model of top-down attention on Neurogrid", Center for Excellence in Education, Science, and Technology (CELEST), Boston University, Boston MA. 2012
12. "Efficient high-performance computing for large-scale brain simulations using neuromorphic chips", Qualcomm Corporation, San Diego CA 2011
13. "Neuromorphics", Northern California Science Writers Association, Burlingame CA. 2011
14. "Neurogrid: Emulating a million neurons in the cortex", Computation and Neural Systems Program, Caltech, Pasadena CA 2011
15. "Neurogrid: Emulating a million neurons in the cortex", Department of Electronic Engineering, Osaka University, Osaka JAPAN. 2010
16. "Modeling the brain with neuromorphic chips", PARC Forum Speaker Series, Palo Alto CA. 2010
17. "Modeling the brain with neuromorphic chips", Symbolic Systems Program, Stanford University, Palo Alto CA. 2010
18. "Modeling the Brain with Neuromorphic Chips", Bay Area Caltech Alumni Luncheon, Palo Alto CA. 2009
19. "Neurogrid: Emulating a million neurons in the cortex", Institute of Neuroinformatics, University of Zurich and Swiss Federal Institute of Technology (ETH), Zurich SWITZERLAND 2009
20. "Neurogrid: Emulating a million neurons in the cortex", Swartz Initiative for Theoretical Neurobiology, Yale University, New Haven CT. 2009
21. "Neurogrid: Emulating a million neurons in the cortex", Physical Sciences Seminar Series, IBM Watson Research Center, Yorktown Heights NY. 2009
22. "Neurogrid: Emulating a million neurons in the cortex", Redwood Center for Theoretical Neuroscience, University of California, Berkeley CA. 2008
23. "Neurogrid: Emulating a million neurons in the cortex", IBM Almaden Research Center, San Jose CA. 2008
24. "Emulating the brain in silicon", Quantum Science Research Group, HP Labs, Palo Alto CA. 2007
25. "Neurogrid: Emulating a million neurons in the cortex", Neuroscience and Cognitive Science Program Colloquium, University of Maryland, College Park MD. 2007

26. "Neurogrid: Emulating a million neurons in the cortex", Neuroengineering Seminar Series, Biomedical Engineering Dept., Yale University, New Haven CT 2007
27. "Neurogrid: Emulating a million neurons in the cortex", Distinguished Lecturer Series, Dept. of Electrical Engineering and Neurosciences Program, University of Southern California, Los Angeles CA. 2007
28. "The technology behind Neurogrid", Electrical Engineering Seminar, Dept. of Electrical Engineering, University of Southern California, Los Angeles CA. 2007
29. "Metaelectronics: Self-configuring neuromorphic systems", Lockheed Martin Advanced Technology Center, Palo Alto CA. 2006
30. "Neurogrid: Emulating a million neurons in the cortex", Air Force Research Lab Chief Scientist's Seminar, Rome, NY. 2006
31. "From local circuits to cortical maps: Modeling V1 in silicon", Department of Physiology and Biophysics, Mt. Sinai School of Medicine, New York NY. 2005
32. "Metamorphing: Self-configuring neuromorphic electronic systems", Bioengineering Dept., Stanford University, Palo Alto CA. 2005
33. "Word-serial address-events for multichip systems", *Microsystems Group*, Electrical and Computer Engineering Dept., Johns Hopkins University, Baltimore MD. 2004
34. "From local circuits to cortical maps: Modeling V1 in silicon", Bodian Seminar Series, *The Mind/Brain Institute*, Johns Hopkins University, Baltimore MD. 2004
35. "A recurrent model of orientation maps with simple and complex cells", *The Helmholtz Club*, University of California, Faculty Club, Irvine CA. 2003
36. "Self-reconfigurable neuromorphic electronics", *Hong Kong University of Science and Technology*, Departments of Biology, Biochemistry, and Electrical & Electronic Engineering, HONG KONG 2003
37. "Self-configuring neuromorphic chips through epigenesis", *Carnegie-Mellon University*, Biological Sciences Dept., Pittsburgh PA 2003
38. "Chips that rewire themselves", *University of Pennsylvania*, Chemical Engineering Dept., Philadelphia PA 2003
39. "A silicon retina with parallel pathways", *University of California*, Dept. of Neuroscience, San Francisco CA 2002
40. "Retinomorphic Vision Chips for Ocular Implants", *Johns Hopkins University*, Dept of Biomedical Engineering, Baltimore MD 2001
41. "Retinomorphic Vision Chips for Ocular Implants", *University of Pennsylvania*, Dept of Neurosurgery, Philadelphia PA 2001
42. "Learning as you grow: Toward Anatomical Plasticity in Silicon", *University of Pennsylvania*, Biochemistry Seminar Series, Philadelphia PA 2001
43. "Morphing the Retina: Neural Circuits in Silicon Chips", *Cornell University*, Electrical and Computer Engineering, Ithaca NY 2000
44. "Morphing the Retina: From Neural Circuits to Silicon Chips", *University of Maryland*, Biology Dept., College Park MD 2000

45. "Retinomorph Vision Systems: Reverse Engineering the Vertebrate Retina", 1997
University of Pennsylvania, Bioengineering Dept., Philadelphia PA
46. "Retinomorph Vision Systems: Reverse Engineering the Vertebrate Retina", 1996
California Institute of Technology, Computer Science Dept., Pasadena CA
47. "Retinomorph Vision Systems: Reverse Engineering the Vertebrate Retina", 1996
Massachusetts Institute of Technology, EECS Dept., Boston MA
48. "Retinomorph Vision Systems: Reverse Engineering the Vertebrate Retina", 1996
Columbia University, Electrical Engineering Dept., New York NY
49. "Retinomorph Vision Systems: Reverse Engineering the Vertebrate Retina", *IBM* 1996
Watson Research Center, Yorktown Heights NY
50. "Retinomorph Vision Systems: Reverse Engineering the Vertebrate Retina", 1996
Lucent Technologies Research, Murray Hill NJ
51. "Retinomorph Vision Systems", *Cambridge University*, Zoology Dept., 1996
Cambridge, ENGLAND
52. "Retinomorph Vision Systems", *University of Bonn*, Computer Science Dept. 1996
Bonn, GERMANY
53. "Retinomorph Vision Systems", *Imperial College*, Electrical & Electronic 1996
Engineering Dept., London, ENGLAND
54. "Retinomorph Vision Systems", *University of Oslo*, Oslo, NORWAY 1996
55. "Speed Sensitivity in a Neuromorphic Retina Chip", *University of California*, 1994
Neurosciences Institute, San Diego CA
56. "A Second-Generation Silicon Retina", *Lawrence Livermore Labs*, Livermore CA 1991
57. "Modeling the Distal Retina in Silicon", *University of California*, Retinal 1991
Neurobiology Group, Berkeley CA

Workshops and Retreats (Invited)

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| 1. | "Neuromorphic Chips: Combining Analog Computation with Digital Communication", <i>Frontiers in Neuromorphics Workshop</i> , University of California, Los Angeles. | 2016 |
| 2. | "Neuromorphic Chips: Combining Analog Computation with Digital Communication", <i>Columbia Workshop on Brain Circuits, Memory and Computation</i> , Columbia University, New York NY. | 2016 |
| 3. | "Neuromorphic Hardware: Design and Applications", DAC Workshop on Alternative Computing in the Nanoscale Era, San Francisco CA. | 2014 |
| 4. | "Designing and Building Large-Scale Neuromorphic Systems", <i>BioCircuits Institute MURI Winter School</i> , UCSD, San Diego CA. | 2014 |
| 5. | "Neuromorphic Architectures: Neurogrid and Beyond", <i>Joint EU-US Workshop on Cortical Processors</i> , Heildelberg GERMANY. | 2013 |
| 6. | "Neuromorphic Architectures", <i>DARPA Cortical Processor Workshop</i> , Millbrae CA. | 2013 |

7. “Special-Purpose Platforms for Large-Scale Neural Modeling”, *NIH-ACD BRAIN Working Group Meeting on Theory, Computation, and Big Data*, Boston MA. 2013
8. “From neuromorphic neural systems to cognitive behaving systems”, *The 2013 CapoCaccia Cognitive Neuromorphic Engineering Workshop*, Capo Caccia ITALY. 2013
9. “Neurogrid: A hybrid analog-digital platform for simulating large-scale neural models”, *NERF Neurotechnology Symposium*, IMEC, Heverlee BELGIUM. 2013
10. “How Neurogrid Works”, *Computational Systems Neuroscience (Cosyne) Workshop on Understanding the Brain by Building One*, Snowbird UT. 2013
11. “Neurogrid: Simulating a million neurons and a billion synapses on sixteen neuromorphic chips”, Bioengineering Dept. Retreat, University of California, Berkeley, Asilomar CA. 2012
12. “Simulating the brain with neuromorphic chips”, *Kavli Futures Symposium III: Real Problems for Imagined Computers*, Tromso NORWAY. 2010
13. “Neurogrid: Emulating a million neurons in the cortex”, *Novel Ways of Computing*, DARPA-DSRC Workshop, Stanford CA. 2009
14. “Neurogrid: Emulating a million neurons in the cortex”, Intel Workshop on *Massively Parallel Adaptive Computing*, Portland OR. 2009
15. “Analog Computing”, *Kavli Futures Symposium on Computing*, San Carlos, COSTA RICA 2009
16. “Vision and memory: Recurrent models”, *Neuroscience Retreat*, Neuroscience Program at Stanford University, Monterey CA. 2007
17. “Outperforming supercomputers with neuromorphic hardware”, *Electronic Cortex Workshop*, Defense Sciences Office, DARPA, Arlington VA. 2007
18. “Open questions in learning: Why hardware needs wetware (not theory)”, *Future Challenges for the Science and Engineering of Learning Workshop*, NSF, Arlington VA. 2007
19. “How to outperform a supercomputer with neuromorphic chips”, *Neuromorphic Engineering Workshop*, Telluride CO 2007
20. “Neurogrid: Emulating a million neurons in the cortex”, *Neurosciences Institute at Stanford (NIS) Retreat*, Asilomar CA. 2007
21. “Neurogrid: Emulating a million neurons in the cortex”, *Grand Challenges in Neural Computation Workshop*, Center for Non-Linear Studies, Los Alamos National Laboratory and Advanced Studies Institute, University of New Mexico, La Posada de Santa Fe, Santa Fe NM. 2007
22. “Neurogrid: Emulating a million neurons in the cortex”, *Multi-level Brain Modeling Workshop*, UCSD and Rancho Santa Fe CA 2006
23. “Ultra large-scale neuromorphic systems”, *A NeuroSilicon Workshop*, Portland State University, Portland OR 2006
24. “Neuromorphic platforms”, *OIDA Roadmap Forum: Artificial Vision Systems*, Boston MA 2006

25. "Neurogrid: Emulating a million neurons in the cortex", *Neuromorphic Engineering Workshop*, Telluride CO 2006
26. "Analog is not neuromorphic: In praise of mismatch", *Neuromorphic Engineering Workshop*, Telluride CO 2006
27. "Learning in silicon: Timing is everything", *Neuromorphic Engineering Workshop*, Telluride CO 2005
28. "How to build a brain", *Packard Fellows Meeting*, Monterey CA 2004
29. "Word-serial address-events for multichip systems", *Neuromorphic Engineering Workshop*, Telluride CO 2004
30. "From local circuits to cortical maps: Modeling V1 in silicon", *Early Cognitive Vision Workshop*, Isle of Skye, SCOTLAND 2004
31. "A 'Neurons that fire together wire together' chip", *Workshop on Optimization and Constraints in the Evolution of Brain Design*, The Banbury Center, Cold Spring Harbor Laboratory, NY 2003
32. "Wiring feature maps by following gradients: Silicon model", *Neuromorphic Engineering Workshop*, Telluride CO 2003
33. "Orientation hypercolumns in visual cortex: Single chip model", *Neuromorphic Engineering Workshop*, Telluride CO 2003
34. "From local circuits to cortical maps", *Sloan-Swartz Foundation Workshop on Neural Circuits*, The Banbury Center, Cold Spring Harbor Laboratory, NY 2003
35. "Silicon Growth Cones: Wiring Together Neurons that Fire Together", *Neuromorphic Engineering Workshop*, Telluride CO 2002
36. "A Retinomorph Chip with Four Ganglion-Cell Types", *Neuromorphic Engineering Workshop*, Telluride CO 2002
37. "Learning where to go: Anatomical Plasticity in Silicon", *Neuromorphic Engineering Workshop*, Telluride CO 2001
38. "A Retinomorph Chip with Four Ganglion-Cell Types", *Neuromorphic Engineering Workshop*, Telluride CO 2001
39. "Neuromorphic Computation *in Silico*", *Joint NSF-DOE Workshop on Biological Information Processing*, Clemson SA 2001
40. "Learning as you grow: Anatomical Plasticity in Silicon", *Packard Fellows Meeting*, Monterey CA 2000
41. "Morphing the Brain: *In Silico* Neural Circuits", *NSF Workshop on Biological Computation*, Washington DC 2000
42. "Retinomorph Vision Chips for Ocular Implants", *Neuromorphic Engineering Workshop*, Telluride CO 2000
43. "Retinomorph Vision Chips for Ocular Implants", *JSPS Workshop on Design and Fabrication of Neural Prostheses*, Shizouka JAPAN 1999
44. "Morphing the Retina", *Neuromorphic Engineering Workshop*, Telluride CO 1999

45. “Toward a Retinal Prosthesis”, *Penn Institute of Medicine and Engineering Retreat*, Philadelphia PA 1999
46. “Multichip Neuromorphic Visual Motion Sensing”, *Neuromorphic Engineering Workshop*, Telluride CO 1998
47. “Multichip Large-Scale Neuromorphic Systems”, *Neuromorphic Engineering Workshop*, Telluride CO 1997
48. “Retinomorphic Vision Systems”, *JASON Summer Study Group*, La Jolla CA 1996
49. “Retinomorphic Chips”, *NASA Workshop: From Neurons to Nanotechnology*, Moffet Field CA 1995

Personal	
<i>Birth Place and Date:</i> Accra, GHANA	22 September 1964
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